S3C49F9X User's Manual
(Compact Flash Controller)

Samsung Electronics Co.,LTD
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1 PRODUCT OVERVIEW

Samsung's S3C49F9X is NAND flash memory controller which can control flash memories as solid state disk. It provides PC Card ATA/IDE interface, host and flash transfer rates up to 20.0MB/S. S3C49F9X can control flash memory maximum 10 pieces if use the 32M,64M,128M,512Mbit and can control flash memory maximum 8 pieces if use the 1Gbit. The device is designed using 0.35-um CMOS process, housed in a 100-TQFP package. It supports operation in both 5.0V and 3.3V.

An outstanding feature of the S3C49F9X flash disk controller is its CPU core: the ARM7TDMI 16/32-bit RISC processor, designed by Advanced RISC Machine (ARM), Ltd. The ARM core is a low-power, general purpose, microprocessor macro-cell that was developed for use in application-specific and customer-specific intergrated circuit. It is simple, elegant, and fully static design is particularly suitable for cost and power sensitive application

1.1 Features

- PC Card-ATA/True IDE/CompactFlash compatible host interface
- Automatic sensing of PC Card ATA and 68-pin IDE
- Included 256-byte CIS RAM
- Five PC Card ATA addressing modes
- Host data transfer rate : 20MB/S
- Flash data transfer rate : 10MB/S
- Host Interface : 8/16-bit Access
- Flash Interface : 8-bit Access
- Support 3 power save mode : stop/idle/active
- Support up to 10 flash memories
- Support 32/64/128/256/512Mbit,1Gbit NAND flash memory made by Samsung

NAND Flash Density	Min. / Max. Capacity (number of flash)
32Mb, 64Mb, 128Mb, 256Mb, 512Mb	4MB / 512MB (Up to 10ea)
1Gb	128MB/1GB (Up to 8ea)

- Auto power down function
- ECC function
- Available 100-pin TQFP
- Operating Voltage : 3.3V to 5.0V

Microprocessor Architecture

- 16/32-bit RISC architecture

- Efficient and powerful ARM7TDMI CPU core

- Cost-effective JTAG based debug solution

System Manager

- 512-Kbyte virtually addressable memory space

- Support 8/16-bit external bus for SRAM/ROM

- Programmable external memory access time

- Included 32-Kbytes internal ROM

- Included 8-Kbytes internal SRAM

DMA Controller

- Two-channel, general-purpose DMA controller

- Memory to memory, PCMCIA to/from memory
   data transfers without CPU Intervention

- Support for 8/16-bit data transfers

- Increment or decrement of source or
   destination address

Programmable Timer

- 1-channel 16-bit programmable timer

Interrupts

- 8 interrupt sources

- Normal or fast interrupt modes (IRQ, FIQ)

PC-Card/ATA Interface

- Include 256-Bytes SRAM for CIS

- Support memory and I/O addressing mode

- Support True IDE mode

- 1-bit ECC

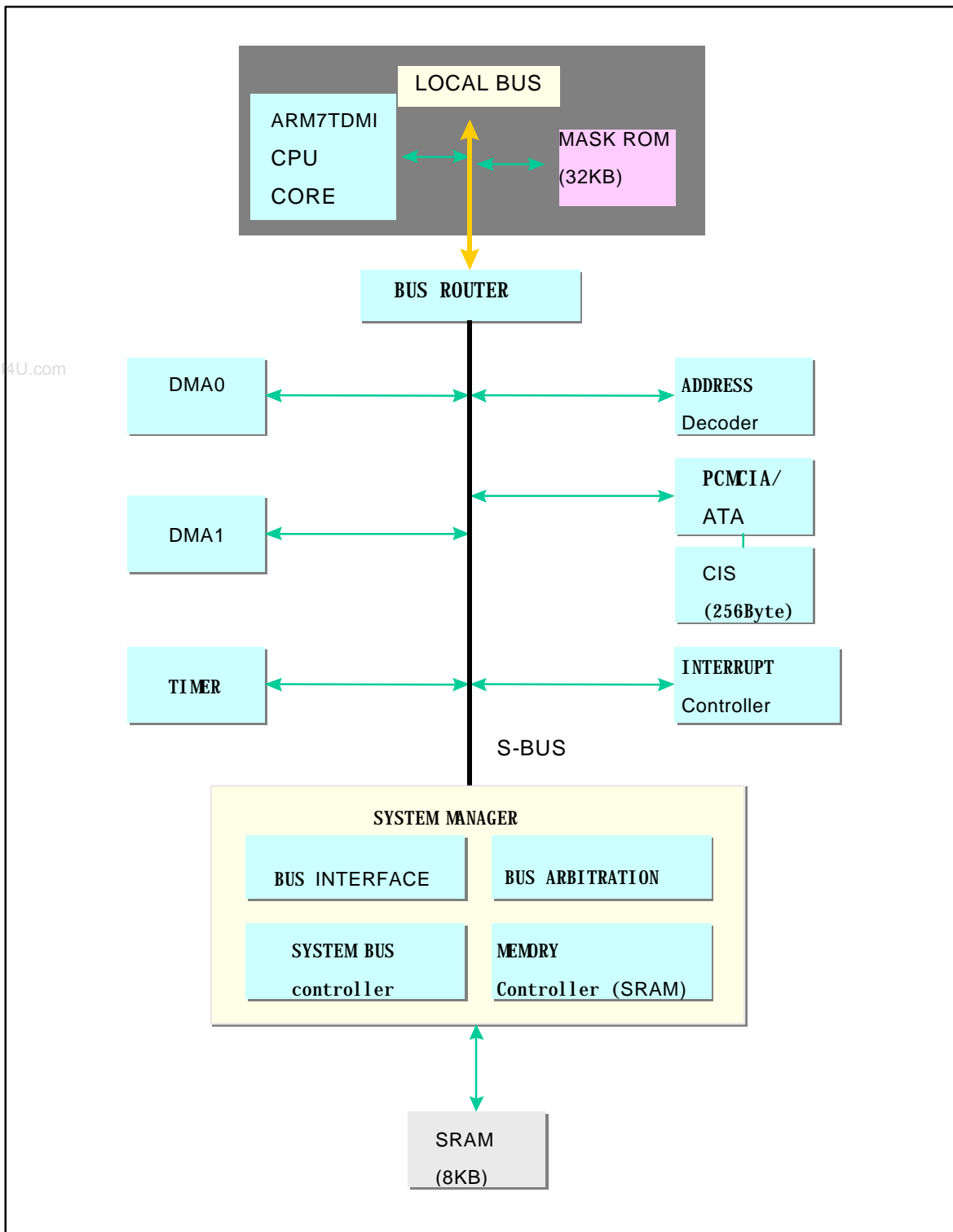**Operating Voltage Range**

- 3.3 to 5.0 volts

Operating Frequency

- Up to 20MHz

Package Type

- 100-TQFP

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1.2 Block Diagram

2 PIN INFORMATION

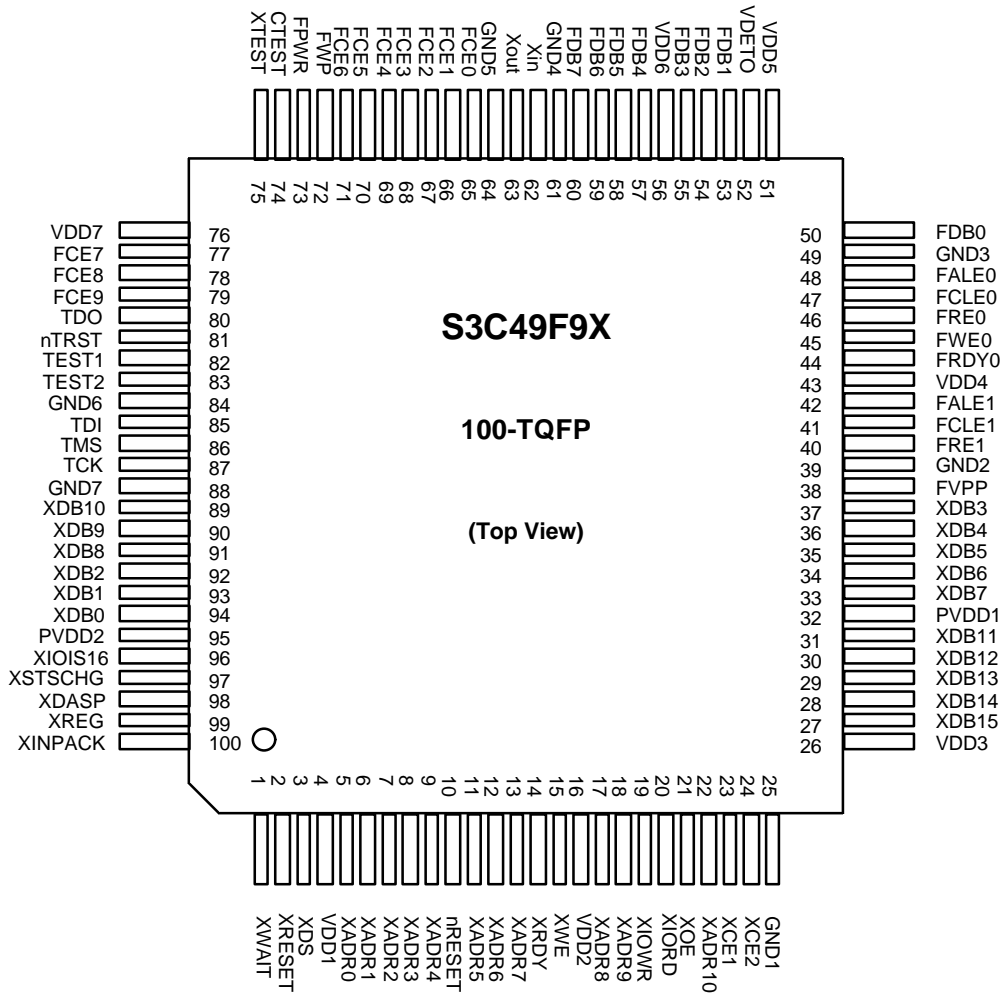## 2.1 Controller Package Drawing

Figure 2-1 S3C49F9X Pin Assignment

2.2 Controller Pin Assignments and Pin type

Table 2-1 Controller Pin Assignments

Pin Number	Signal Name	Pin Type	I/O Type	Function
1	XWAIT	O	O1	Wait of PCMCIA
2	XRESET	I	I1	Write protect of flash chips for flash bus 0,1
3	XDS	I	I5	Device select for IDE
4	VDD1	-	-	System power
5	XADR0	I	I1	Address bus of PCMCIA
6	XADR1	I	I1	Address bus of PCMCIA
7	XADR2	I	I1	Address bus of PCMCIA
8	XADR3	I	I1	Address bus of PCMCIA
9	XADR4	I	I1	Address bus of PCMCIA
10	nRESET	I	I3	System power reset
11	XADR5	I	I1	Address bus of PCMCIA
12	XADR6	I	I1	Address bus of PCMCIA
13	XADR7	I	I1	Address bus of PCMCIA
14	XRDY	O	O1	Ready(IREQ) of PCMCIA
15	XWE	I	I2	Write enable of PCMCIA
16	VDD2	-	-	System power
17	XADR8	I	I1	Address bus of PCMCIA
18	XADR9	I	I1	Address bus of PCMCIA
19	XIOWR	I	I2	IOWR of PCMCIA
20	XIORD	I	I2	IORD of PCMCIA
21	XOE	I	I2	Output enable of PCMCIA
22	XADR10	I	I1	Address bus of PCMCIA
23	XCE1	I	I2	Card enable1 of PCMCIA
24	XCE2	I	I2	Card enable2 of PCMCIA
25	GND1	-	-	Ground
26	VDD3	-	-	System power
27	XDB15	I/O	B1	Data bus of PCMCIA
28	XDB14	I/O	B1	Data bus of PCMCIA
29	XDB13	I/O	B1	Data bus of PCMCIA
30	XDB12	I/O	B1	Data bus of PCMCIA
31	XDB11	I/O	B1	Data bus of PCMCIA
32	PVDD1	-	-	PCMCIA power
33	XDB7	I/O	B1	Data bus of PCMCIA
34	XDB6	I/O	B1	Data bus of PCMCIA
35	XDB5	I/O	B1	Data bus of PCMCIA
36	XDB4	I/O	B1	Data bus of PCMCIA
37	XDB3	I/O	B1	Data bus of PCMCIA

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38	FVPP	-	-	High voltage power for OTP

Table 2-1 Controller Pin Assignments (Cont.)

Pin Number	Signal Name	Pin Type	I/O Type	Function
39	GND2	-	-	Ground
40	FRE1	I/O	B9	Read enable flash chips of flash bus1
41	FCLE1	I/O	B5	Command latch enable of flash chips of flash bus1
42	FALE1	I/O	B5	Address latch enable of flash chips of flash bus1
43	VDD4	-	-	System power
44	FRDY0	I/O	B5	Ready signal of flash chips of flash bus0
45	FWE0	I/O	B9	Write enable of flash chips of flash bus0
46	FRE0	I/O	B9	Read enable flash chips of flash bus0
47	FCLE0	I/O	B5	Command latch enable of flash chips of flash bus1
48	FALE0	I/O	B5	Address latch enable of flash chips of flash bus1
49	GND3	-	-	Ground
50	FDB0	I/O	B7	I/O of flash chips of flash bus0,1
51	VDD5	-	-	System power
52	VDETO	O	O2	Voltage detect output
53	FDB1	I/O	B7	I/O of flash chips of flash bus0,1
54	FDB2	I/O	B7	I/O of flash chips of flash bus0,1
55	FDB3	I/O	B7	I/O of flash chips of flash bus0,1
56	VDD6	-	-	System power
57	FDB4	I/O	B7	I/O of flash chips of flash bus0,1
58	FDB5	I/O	B7	I/O of flash chips of flash bus0,1
59	FDB6	I/O	B7	I/O of flash chips of flash bus0,1
60	FDB7	I/O	B7	I/O of flash chips of flash bus0,1
61	GND4	-	-	Ground
62	XI	-	OSC	Input clock
63	XO	-	OSC	Output clock
64	GND5	-	-	Ground
65	FCE0	I/O	B3	Chip enable 0 of flash chips of flash bus0,1
66	FCE1	I/O	B3	Chip enable 1 of flash chips of flash bus0,1
67	FCE2	I/O	B3	Chip enable 2 of flash chips of flash bus0,1
68	FCE3	I/O	B3	Chip enable 3 of flash chips of flash bus0,1
69	FCE4	I/O	B3	Chip enable 4 of flash chips of flash bus0,1
70	FCE5	I/O	B3	Chip enable 5 of flash chips of flash bus0,1
71	FCE6	I/O	B3	Chip enable 6 of flash chips of flash bus0,1
72	FWP	I/O	B5	Write protect of flash chips of flash bus 0, 1
73	FPWR	O	O2	Power control signal for flash memory
74	CTEST	I	I4	Core test mode select signal

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75	XTEST	I	I4	Test input for test mode

Table 2-1 Controller Pin Assignments (Cont.)

Pin Number	Signal Name	Pin Type	I/O Type	Function
76	VDD7	-	-	System power
77	FCE7	I/O	B3	Chip enable 7 of flash chips of flash bus0,1
78	FCE8	I/O	B3	Chip enable 8 of flash chips of flash bus0,1
79	FCE9	I/O	B3	Chip enable 9 of flash chips of flash bus0,1
80	TDO	O	O2	Test data output for JTAG
81	nTRST	I	I4	Test reset for JTAG
82	TEST1	I	I4	OTP mode select signal 1
83	TEST2	I	I4	OTP mode select signal 2
84	GND6	-	-	Ground
85	TDI	I	I4	Test data input for JTAG
86	TMS	I	I4	Test mode select for JTAG
87	TCK	I	I4	Test clock for JTAG
88	GND7	-	-	Ground
89	XDB10	I/O	B1	Data bus of PCMCIA
90	XDB9	I/O	B1	Data bus of PCMCIA
91	XDB8	I/O	B1	Data bus of PCMCIA
92	XDB2	I/O	B1	Data bus of PCMCIA
93	XDB1	I/O	B1	Data bus of PCMCIA
94	XDB0	I/O	B1	Data bus of PCMCIA
95	PVDD2	-	-	PCMCIA power
96	XIOIS16	I/O	B1	IOIS16 of PCMCIA
97	XSTSCHG	I/O	B1	STSCHG of PCMCIA
98	XDASP	I/O	B4	DASP for IDE
99	XREG	I	I2	REG of PCMCIA
100	XINPACK	O	O1	INPACK of PCMCIA

Table 2-2 I/O Type Description

I/O Type	Pad Type	Description
I1	PVIL3	3.3V TTL schmitt trigger level PCMCIA LIN input buffer
I2	PVILU3	3.3V TTL schmitt trigger level PCMCIA LIN input buffer with pull-up register
I3	PIS	CMOS schmitt trigger level input buffer
I4	PIC	CMOS level input buffer
I5	PICU	CMOS level input buffer with pull-up register
I6	PICD	CMOS level input buffer with pull-down register
I7	PVILD3	3.3V TTL schmitt trigger level PCMCIA LIN input buffer with pull-down register
O1	PVOB43	3.3V 4mA PCMCIA output buffer without SRC
O2	POD4	4mA open drain output buffer
O3	POB4	4mA Normal output buffer
O4	POB4SM	4mA Normal output buffer with medium slew-rate control
O5	POB16SM	16mA Normal output buffer with medium slew-rate control
O6	POB12	12mA Normal output buffer
B1	PVBTT43	3.3V 4mA PCMCIA LIN bi-directional buffer without SRC
B2	PBCT4	CMOS level input buffer and 4mA tri-state output buffer
B3	PBCT4SM	CMOS level input buffer and 4mA tri-state output buffer with medium slew-rate control
B4	PBCUT4SM	CMOS level input buffer with pull-up register and 4mA tri-state output buffer with medium slew-rate control
B5	PBCT8SM	CMOS level input buffer and 8mA tri-state output buffer with medium slew-rate control
B6	PBCUT8SM	CMOS level input buffer with pull-up register and 8mA tri-state output buffer with medium slew-rate control
B7	PBCDT8	CMOS level input buffer with pull-down register and 8mA tri-state output buffer
B8	PBSDT4SM	CMOS schmitt trigger level input buffer with pull-down register and 4mA tri-state output buffer with medium slew-rate control
B9	PBCT16SM	CMOS level input buffer and 16mA tri-state output buffer with medium slew-rate control
B10	PVBTD43	3.3V 4mA PCMCIA LIN bi-directional buffer without SRC with pull-down register
OSC	PSOSCM26	Oscillator cell with enable and register

2.3 Pin description for host interface

Table 2-3 Pin description for host interface

Signal Name	100-Pin Number	I/O	Description
XARD0	5		ADDRESS BUS[10:0] : These address lines along with the –REG signal are used to select the following: The I/O port address registers within the PC Storage Card, the memory mapped port address registers within the PC Storage Card, a byte in the Card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal in PC Card I/O mode. In True IDE Mode only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
XARD1	6		
XARD2	7		
XARD3	8		
XARD4	9		
XARD5	11	I	
XARD6	12		
XARD7	13		
XARD8	17		
XARD9	18		
XARD10	22		
XDB0	94		DATA BUS[15:0] : These lines carry the Data, Commands and Status information between the host and the controller. XDB0 is the LSB of the even byte of the word. XDB8 is the LSB of the odd byte of the word. This signal is the same as the PC Card memory mode signal in PC Card I/O mode. In True IDE mode, all Task File operations occur in byte mode on the low order bus XDB0-XDB7 while all data transfers are 16 bit using XDB0-XDB15.
XDB1	93		
XDB2	92		
XDB3	37		
XDB4	36		
XDB5	35		
XDB6	34		
XDB7	33	I/O	
XDB8	91		
XDB9	90		
XDB10	89		
XDB11	31		
XDB12	30		
XDB13	29		
XDB14	28		
XDB15	27		
XREG	99	I	ATTRIBUTE MEMORY AREA SELECTION : This signal is used during memory cycles to distinguish between common memory and register (Attribute) memory accesses. High for Common memory, low for attribute memory. The signal must also be active (low) during I/O cycles when the I/O address is on the Bus. In True IDE mode, this input signal is not used and should be connected to VCC by the host.

Table 2-3 Pin description for host interface(Cont.)

Signal Name	100-Pin Number	I/O	Description
XCE1	23	I	CARD ENABLE : These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multi-plexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on XDB0-XDB7. See tables 3-7,3-8,4-3 and 4-4. This signal is the same as the PC card memory mode signal in PC Card I/O mode. In the True IDE mode, CS0 is the chip select for the task file registers while CS1 is used to select the alternate status register and the device control register.
XCE2	24	I	
XOE	21	I	OUTPUT ENABLE : This is an output enable strobe generated by the host interface. It is used to read data from the PC Card in memory mode and to read the CIS and configuration registers. In PC Card I/O mode, this signal is used to read the CIS and configuration registers. To enable True IDE mode this input should be grounded by the host.
XWE	15	I	WRITE ENABLE : This is a signal driven by the host and used for strobing memory write data to the registers of the PC Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O mode, this signal is used for writing the configuration registers. In True IDE mode, this input signal is not used and should be connected to VCC by the host.
XWAIT	1	O	WAIT : The -WAIT signal is driven low by the PC Card to signal the host to delay completion of a memory or I/O cycle that is in progress. IORDY : In True IDE mode, this output signal may be used as IORDY.

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Table 2-3 Pin description for host interface(Cont.)

Signal Name	100-Pin Number	I/O	Description
XIOIS16	96	I/O	I/O PORT IS 16 BITS : Memory mode - The PC Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O operation - When the PC Card is configured for I/O operation pin 24 is used for the -I/O selected is 16-Bit Port (-IOIS16) function. A low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE mode, this output signal is asserted low when this device is expecting a word data transfer cycle.
XINPACK	100	O	INPUT PORT ACKNOWLEDGE : This signal is not used in memory mode. The Input acknowledge signal is asserted by the PC Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the PC Card and the CPU. In True IDE mode, this output signal is not used and should be connected at the host.
XRDY/	14	O	READY/BUSY : In memory mode, this signal is set high when the PC Card is ready to accept a new data transfer operation and held low when the card is busy. The host memory card socket must provide a pull-up resistor. At power up and at reset, the RDY/-BSY signal is held low (busy) until the PC Card has completed its power up or reset function. No access of any type should be made to the PC Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The PC Card has been powered up with +RESET continuously disconnected or asserted. I/O operation - After the PC Card has been configured for I/O operation, this signal is used as Interrupt request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE mode, this signal is the active high Interrupt request to the host.

Table 2-3 Pin description for host interface(Cont.)

Signal Name	100-Pin Number	I/O	Description
XIORD	20	I	I/O READ : This signal is not used in memory mode. This is an I/O read strobe generated by the host. This signal gates I/O data onto the bus from the PC Card when the card is configured to use the I/O interface. In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
XIOWR	19	I	I/O WRITE : This signal is not used in memory mode. The I/O write strobe pulse is used to clock I/O data on the card data bus into the PC Card controller registers when the PC Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge). In True IDE mode, this signal has the same function as in PC Card I/O Mode.
XSTSCHG	97	I/O	STATUS CHANGED : This signal is asserted high as the BVD1 signal since a battery is not used with this product. This signal is asserted low to alert the host to changes in the RDY/-BSY and write protect states, while the I/O interface is configured. Its use is controlled by the Card config and status In the True IDE mode, this input / output is the pass diagnostic signal in the Master / Slave handshake protocol.
XDS	3	I	CARD SELECT : In True IDE mode, this signal is used for configure this device as a master or slave. When it is grounded , the device is configured as a master. When this signal is open, the device is configured as a slave. In I/O and memory mode, this signal is not used.
XRESET	2	I	RESET : When the pin is high, this signal resets the PC Card. The PC Card is reset only at Power up if this pin is left high or open from power-up. The PC Card is also reset when the soft reset bit in the Card Configuration Option Register is set. In the True IDE mode, this input pin is the active low hardware reset from the host.

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Table 2-3 Pin description for host interface(Cont.)

Signal Name	100-Pin Number	I/O	Description
XDASP	98	I/O	This output line is always driven to a high state in memory mode since a battery is not required for this product. This output line is always driven to a high state in I/O mode since this product does not support the audio function. In the True IDE mode, this input/output is the disk active/slave present signal in the Master/Slave handshake protocol.
XP55	-	I	Input for inverter
XP56	-	O	Output for inverter
VDEOT	52	O	Voltage detect output
XTEST	75	I	Test input for test mode

2.4 Pin Assignment for Flash Memory Interface

Table 2-4 Pin description for Flash memory interface

Signal Name	100-Pin Number	I/O	Description
FDB0	50		FLASH DATA BUS[15:0] : These lines are 16-bit data lines to/from the flash memory chip.
FDB1	53		
FDB2	54		
FDB3	55		
FDB4	57		
FDB5	58		
FDB6	59		
FDB7	60		
FDB8	-	I/O	
FDB9	-		
FDB10	-		
FDB11	-		
FDB12	-		
FDB13	-		
FDB14	-		
FDB15	-		
FRDY0	44	I/O	FLASH READY 0/1 : The signal is used for indicate to the controller, which flash memory is ready to accept a command. FDB0 ~ FDB7 are controlled by FRDY0 signal, FDB8 ~ FDB15 are controlled by FRDY1.
FRDY1	-	I	
FALE0	48	I/O	FLASH ADDRESS LATCH ENABLE 0/1 : When this signal is asserted the controller can send an address to the flash memory by asserting of FWE pin. FDB0 ~ FDB7 are controlled by FALE0 signal, FDB8 ~ FDB15 are controlled by FALE1.
FALE1	42	I/O	
FCLE0	47	I/O	FLASH COMMAND LATCH ENABLE 0/1 : When this signal is asserted, a command can be to the flash memory. FDB0 ~ FDB7 are controlled by FCLE0 signal, FDB8 ~ FDB15 are controlled by FCLE1.
FCLE1	41	I/O	
FRE0	46	I/O	FLASH READ ENABLE 0/1 : This signal is asserted to enable the reading of data from the flash memory. FDB0 ~ FDB7 are controlled by FRE0 signal, FDB8 ~ FDB15 are controlled by FRE1.
FRE1	40	I/O	
FWE0	45	I/O	FALSH WRITE ENABLE 0/1 : When this signal is asserted , the controller can write data to the flash memory. FDB0 ~ FDB7 are controlled by FWE0 signal, FDB8 ~ FDB15 are controlled by FWE1.
FWE1	-	O	

Table 2-4 Pin description for Flash memory interface(Cont.)

Signal Name	100-Pin Number	I/O	Description
FCE0	65		FLASH CHIP ENABLE [9:0] : These lines are flash memory enable signal.
FCE1	66		
FCE2	67		
FCE3	68		
FCE4	69	I/O	
FCE5	70		
FCE6	71		
FCE7	77		
FCE8	78		
FCE9	79		
FWP	72	I/O	Write protect of flash chips of flash bus 0, 1
FPWR	73	O	Power control signal for flash memory

2.5 Pin Assignment for external memory control

Table 2-5 Pin description for external memory interface

Signal Name	100-Pin Number	I/O	Description
ADDR0	-		EXTERNAL MEMORY ADDRESS BUS [16:0] : These signals are address bus to access external memory device as SRAM or ROM.
ADDR1	-		
ADDR2	-		
ADDR3	-		
ADDR4	-		
ADDR5	-		
ADDR6	-		
ADDR7	-		
ADDR8	-	O	
ADDR9	-		
ADDR10	-		
ADDR11	-		
ADDR12	-		
ADDR13	-		
ADDR14	-		
ADDR15	-		
ADDR16	-		
DATA0	-		EXTERNAL MEMORY DATA BUS [7:0] : These signals are data bus to access external memory device as SRAM or ROM.
DATA1	-		
DATA2	-		
DATA3	-		
DATA4	-	I/O	
DATA5	-		
DATA6	-		
DATA7	-		
nRCS	-	O	EXTERNAL ROM CHIP SELECT : When this signal is asserted(low active) , the controller can access the external ROM device.
nSCS	-	O	EXTERNAL SRAM CHIP SELECT : When this signal is asserted(low active) , the controller can access the external SRAM device.
nOE	-	O	OUTPUT ENABLE : This signal is data output enable signal. When an external memory access for ROM/SRAM occurs, this signal controls the output enable port of the specific device.
nWE	-	O	WRITE ENABLE : When an external memory device access for SRAM/ROM occurs, this signal control the write enable port of the specific device.

Table 2-5 Pin description for external memory interface(Cont.)

Signal Name	100-Pin Number	I/O	Description
TCK	87	I	TEST CLOCK : The KS32P49F9X contains internally in-circuit emulation block for debugger mode which use standard JTAG protocol. When the controller go into debugger mode, this signal is provided from external debugger tool.
TMS	86	I	TEST MODE SELECT : In the debugger mode, this signal select test mode. This pin should be held to "1', when do not use the JTAG block.
TDI	85	I	TEST DATA INPUT : In the debugger mode, this signal is used for carry data. from external debugger tool to the controller.
nTRST	81	I	TEST RESET : This signal should be sustained LOW first at the begging of normal operation.
TDO	80	I/O	TEST DATA OUTPUT : In the debugger mode, this signal is used for carry data. from the controller to external debugger tool.
XI	62	OC	INPUT CLOCK : This signal is system clock.
XO	63	OC	OUTPUT CLOCK :
nRESET	-	I	RESET : This pin is system power on reset . A low input will stop all operation within the controller.
SW1	-	I	ROM SELECTION : This pin is used for select ROM. When this signal set "1", the controller access external ROM. When this pin is "0", the controller access internal ROM.
SW0	-	I	FLASH NUMBER OF SELECTION : Basically flash memory can be connected up to 20. But if use the external buffer on pc card , flash memory can be connected up to 32. This signal is used for select number of flash. When this signal is high, can be connected up to 20. In the case of low, can be connected up to 32.
CTEST	74	I	CORE TEST : This signal is used for test CPU(ARM7TDMI) core. When this signal is low(0), the controller operate normal mode. When it is high(1), operate CPU test mode.
CMODE	-	I	INTERRUPT ENABLE : This signal is used for control interrupt signal of CPU, when the signal is set(1), interrupt signal of CPU can be enabled. When this signal is cleared(0), interrupt signal can be disabled.
TEST1	82	I	OTP MODE SELECT : These signals are used for select OTP mode. When OTPMS1 and OTPMS2 are low, the controller operate normal mode. To operate the OTP mode, OTPMS1 and OTPMS2 signal should be set to low and high. The others setting mode are reserved for chip maker.
TEST2	83	I	

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2.6 Power Pin Assignment

Table 2-6 Pin description for power signal

Signal Name	100-Pin Number	I/O	Description
VDD	4,16,26,43,51,56,76	-	System power supply voltage
PVDD	32,95	-	PCMCIA power supply voltage
FVPP	38	-	High voltage power for internal OTP(12.5V)
GND	25,39,49,61,64,84,88	-	Ground

3   INTERFACE BUS TIMMING

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, a direct mapped I/O transfer and a memory access. The two timing sequences are explained in detail in the PCMCIA PC Card Standard. The PC Card conforms to the timing in that reference document.

3.1 Attribute Memory Read Timing Specification

The attribute memory read time is defined as 300ns. Detailed timing specifications are shown in Table 3-1.

Table 3-1 Attribute Memory Read Timing

Parameter	Symbol	IEEE Symbol	300 ns	
			Min ns.	Max ns.
Read Cycle Time	tcR	TAVAV	300	
Address Access Time	ta(A)	TAVQV		300
Card Enable Access Time	ta(CE)	TELQV		300
Output Enable Access Time	ta(OE)	TGLQV		150
Output Disable Time from CE	tdis(CE)	TEHQZ		100
Output Disable Time from OE	tdis(OE)	TGHQZ		100
Address Setup Time	tsu(A)	TAVWL	30	
Output Enable Time from CE	ten(CE)	TELQNZ	5	
Output Enable Time from OE	ten(OE)	TGLQNZ	5	
Data Valid from Address Change	tv(A)	TAXQX	0	

Note.   *All times are in nanosecond. Dout signifies data provided by the PC Card to the system. The –CE signal or both the –OE signal & the -WE signal must be de-asserted between consecutive cycle operation.*
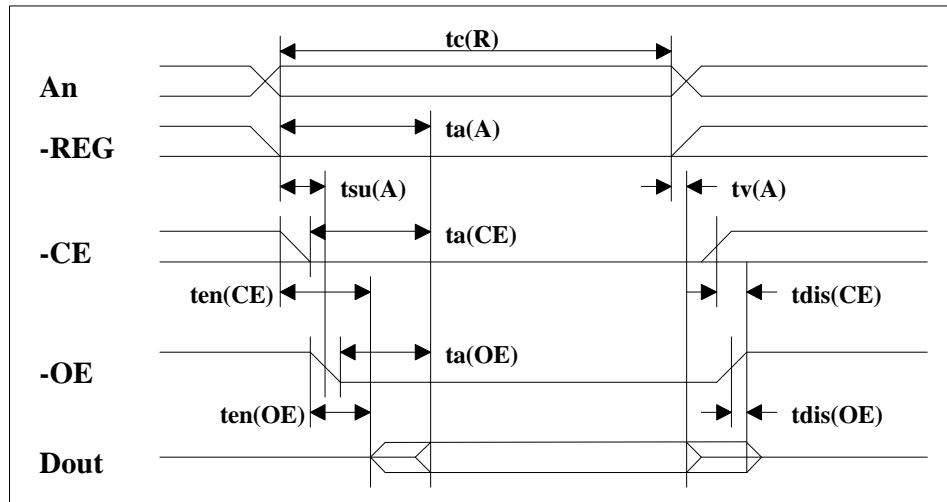
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Figure 3-1 Attribute Memory Read Timing Diagram

3.2 Attribute Memory Write Timing Specification

The attribute memory access time is defined as 250 ns. Detailed timing specifications are shown
in table 3-2.

Note.   *A host cannot write to CIS. This timing is specified only for the write to Configuration Register.*

Table 3-2 Attribute Memory Write Timing

Parameter	Symbol	IEEE Symbol	250 ns	
			Min ns.	Max ns.
Write Cycle Time	tcW	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

Note.   *All times are in nanosecond. Din signifies data provided by the system to the PC Card.*
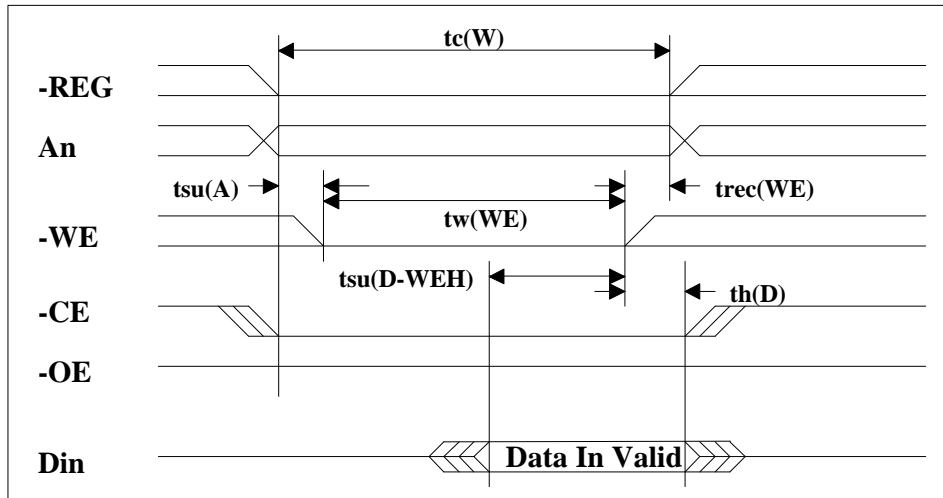

Figure 3-2 Attribute Memory Write Timing Diagram

3.3 Common Memory Read Timing Specification

Table 3-3 Common Memory Read Timing

Parameter	Symbol	IEEE Symbol	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Address Hold Time	th(A)	tGHAX	20	
CE Setup before OE	tsu(CE)	tELGL	0	
CE Hold following OE	th(CE)	tGHEH	20	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35
Data Setup for Wait Release	tv(WT)	tQVWTH		0
Wait Width Time	tw(WT)	tWTLWTH		350

Note.   *The maximum load on -WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds. Dout signifies data provided by the PC Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12s but is intentionally less in this specification.*

Figure 3-3 Common Memory Read Timing Diagram

3.4 Common Memory Write Timing Specification

Table 3-4 Common Memory Write Timing

Parameter	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before WE	tsu(D-WEH)	tDVWH	80	
Data Hold following WE	th(D)	tIWMDX	30	
WE Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
CE Setup before WE	tsu(CE)	tELWL	0	
Write recovery Time	trec(WE)	tWMAX	30	
Address Hold Time	th(A)	tGHAX	20	
CE Hold following WE	th(CE)	tGHEH	20	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35
WE High from Wait Release	tv(WT)	tWTHWH	0	
Wait Width Time	tw(WT)	tWTLWTH		350

Note.   The maximum load on -WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds. Din signifies data provided by the system to the PC Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12s but is intentionally less in this specification.
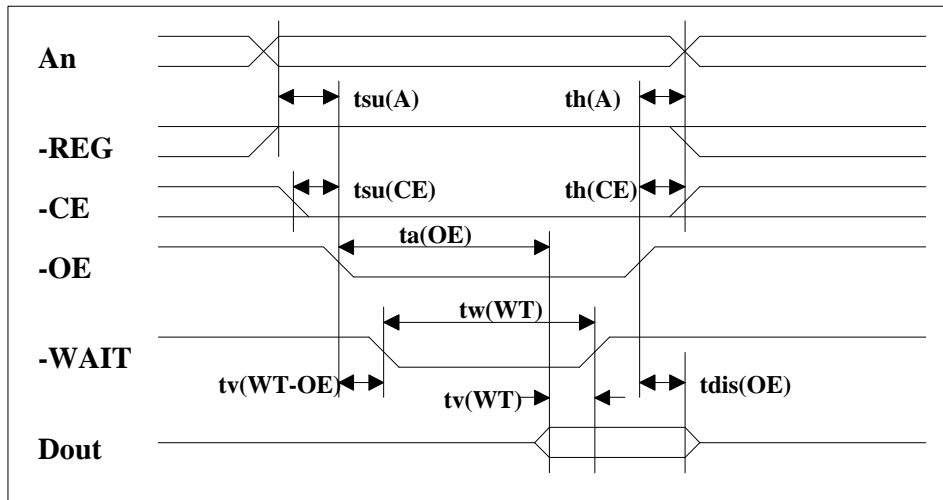

Figure 3-4 Common Memory Write Timing Diagram

3.5 I/O Input (Read) Timing Specification

Table 3-5 I/O Read Timing

Parameter	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL		35
Data Delay from Wait Rising	td(WT)	tWTHQV		0
Wait Width Time	tw(WT)	tWTLWTH		350

Note. *The maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0nsec, but minimum -IORD width must still be met. Dout signifies data provided by the PC Card to the system. The Wait Width time meets the PCMCIA specification of 12s but is intentionally less in this specification.*
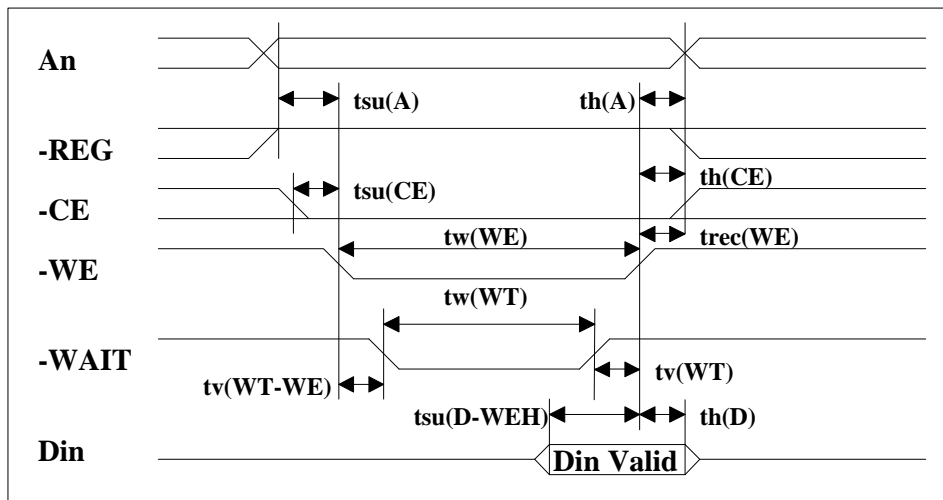

Figure 3-5 I/O Read Timing Diagram

3.6 I/O Output (Write) Timing Specification

Table 3-6 I/O Write Timing

Parameter	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tlWHDX	30	
IOWR Width Time	twIOWR	tlWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tlWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tlWHEH	20	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5	
REG Hold following IOWR	thREG(IOWR)	tlWHRGH	0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IOWR	tdWT(IOWR)	tlWLWTL		35
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0	
Wait Width Time	tw(WT)	tWTLWTH		350

Note.   *The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0nsec, but minimum -IOWR width must still be met. Din signifies data provided by the system to the PC Card. The Wait Width time meets the PCMCIA specification of 12s but is intentionally less in this specification.*
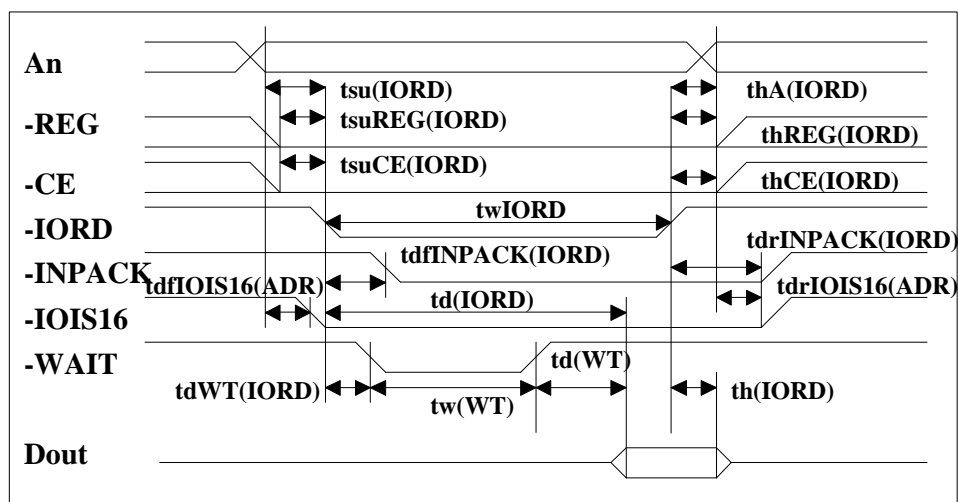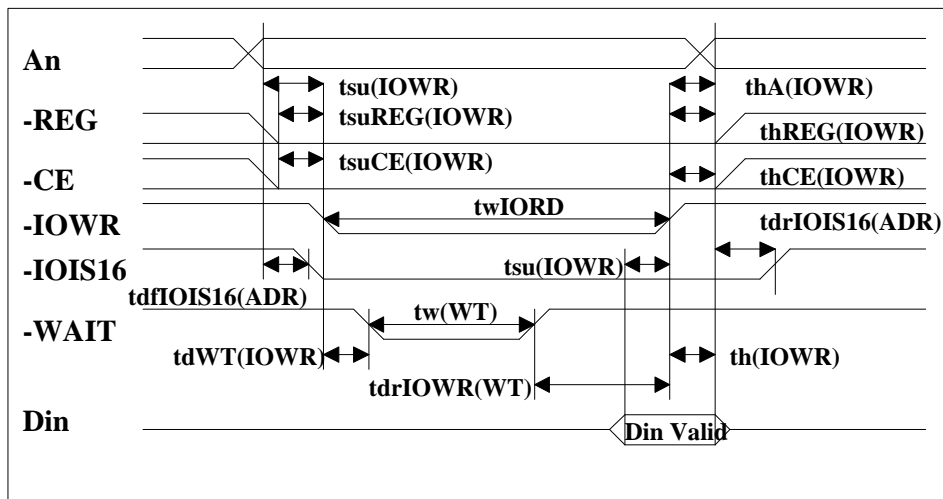

Figure 3-6 I/O Write Timing Diagram

3.7 IDE Mode I/O Input(Read) Timing Specification

Table 3-7 IDE Mode I/O Read Timing

Parameter	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

Note.   *The maximum load on -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0nsec, but minimum -IORD width must still be met. Dout signifies data provided by the PC Card to the system.*
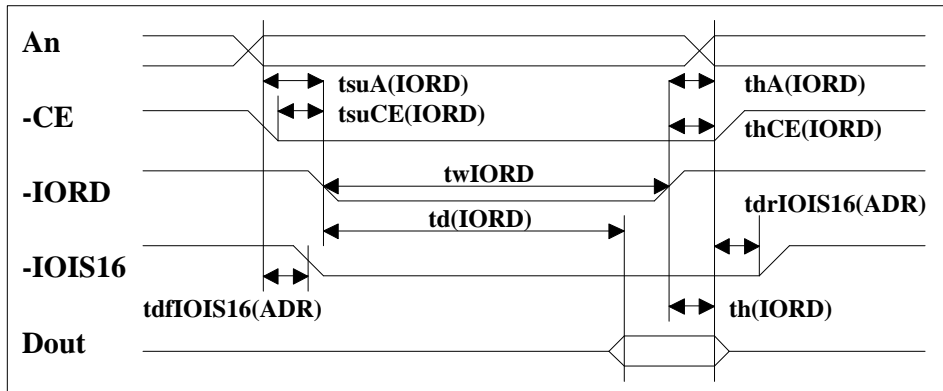
Figure 3-7 IDE Mode I/O Read Timing Diagram

3.8 IDE Mode I/O Output(Write) Timing Specification

Table 3-8 IDE Mode I/O Write Timing

Parameter	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	twIOWR	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

Note.   *The maximum load on -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0nsec, but minimum -IOWR width must still be met. Din signifies data provided by the system to the PC Card.*
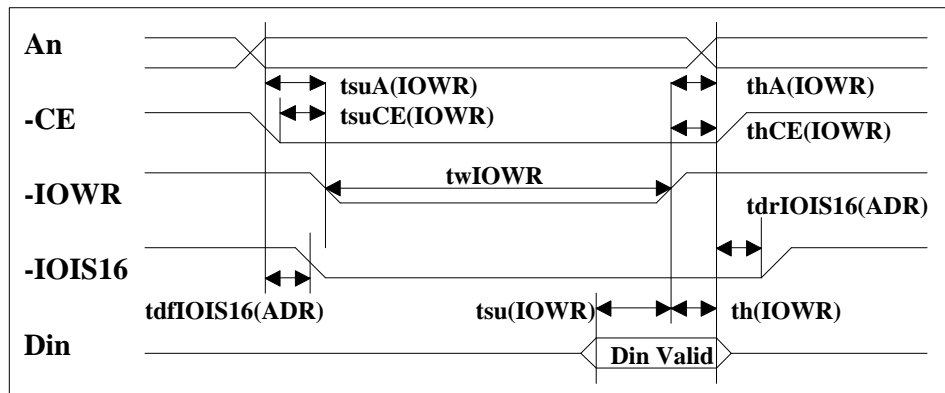
Figure 3-8 I/O Write Timing Diagram

4   CARD CONFIGURATION

The PC Cards are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the PC Card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

Table 4-1 Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	×	×	×	×	×	××	×	×	×	×	Standby
×	0	0	0	1	×	1	××	×	×	×	0	Configuration Registers Read
1	0	1	0	1	×	×	××	×	×	×	×	Common Memory Read(8bit D7-D0)
0	1	1	0	1	×	×	××	×	×	×	×	Common Memory Read(8bit D15-D8)
0	0	1	0	1	×	×	××	×	×	×	0	Common Memory Read(16bit D15-D0)
×	0	0	1	0	×	1	××	×	×	×	0	Configuration Registers Write
1	0	1	1	0	×	×	××	×	×	×	×	Common Memory Write(8bit D7-D0)
0	1	1	1	0	×	×	××	×	×	×	×	Common Memory Write(8bit D15-D8)
0	0	1	1	0	×	×	××	×	×	×	0	Common Memory Write(16bit D15-D0)
×	0	0	0	1	0	0	××	×	×	×	0	Card Information Structure Read
1	0	0	1	0	0	0	××	×	×	×	0	Invalid Access (CIS Write)
1	0	0	0	1	×	×	××	×	×	×	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	×	×	××	×	×	×	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	×	×	××	×	×	×	×	Invalid Access (Odd Attribute Read)
0	1	0	1	0	×	×	××	×	×	×	×	Invalid Access (Odd Attribute Write)

Table 4-2 Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
×	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
×	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
×	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
×	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
×	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
×	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
×	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
×	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Note.   *The location of the card configuration registers should always be read from the CIS since these locations may vary in future products. No writes should be performed to the PC Card attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.*

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4.1 Attribute Memory Function

Attribute memory is a space where PC Card identification and configuration information are stored, and is limited to 8-bit wide accesses only at even addresses. The card configuration registers are also located here. For the attribute memory read function, signals -REG and -OE must be active and -WE inactive during the cycle. As in the main memory read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the attribute memory access. Refer to table 4-3 below for signal states and bus validity for the attribute memory function.

Table 4-3 Attribute Memory Function

Function Mode	-REG	-CE2	-CE1	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	×	H	H	×	×	×	×	High Z	High Z
Read Byte Access CIS (8 bits)	L	H	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (invalid)	L	H	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	H	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	×	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (invalid)	L	L	L	L	×	H	L	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	H	×	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	H	×	H	L	Don't Care	Even Byte

Note   *The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.*

4.2 Configuration Option Register (Address 200h in attribute memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the PC Card.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevIREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET Soft Reset - Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the PC Card in the reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the PC Card in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PCMCIA Soft Reset is considered a hardware reset by the ATA commands. Contrast with software reset in the Device Control Register.

LevIREQ This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when pulse mode is selected. Set to zero (0) by reset.

Conf5 - Conf0 Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the PC Card as shown below.

Note: *Conf5 and Conf4 are reserved and must be written as zero (0)*

Table 4-4 Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	I/O Mapped, 170-177/376-377

4.3 Card Configuration and Status Register (Address 202h in attribute memory)

The Card Configuration and Status Register contains information about the Card's condition.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

Changed   Indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the PC Card is configured for the I/O interface.

SigChg   This bit is set and reset by the host to enable and disable a state-change signal from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the PC Card is configured for I/O.

IOis8   The host sets this bit to a one (1) if the PC Card is to be configured in an 8 bit I/O Mode. The PC Card is always configured for both 8- and 16-bit I/O, so this bit is ignored.

PwrDwn   This bit indicates whether the host requests the PC Card to be in the power saving or active mode. When the bit is one (1), the PC Card enters a power down mode. When zero (0), the host is requesting the PC Card to enter the active mode. The PCMCIA Rdy/-Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The PC Card automatically powers down when it is idle and powers back up when it receives a command.

Int   This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

4.4 Pin Replacement Register (Address 204h in attribute memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	0	0	Rdy/-Bsy	WProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	MWProt

CRdy/-Bsy   This bit is set to one (1) when the bit RRdy/-Bsy changes state. This bit can also be written by the host.

CWProt   This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

Rdy/-Bsy   This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

WProt   This bit is always zero (0) since the PC Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRdy/-Bsy   This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

MWProt   This bit when written acts as a mask for writing the corresponding bit CWProt.

Table 4-5 Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final "C" Bit	Command
	"C" Bit	"M" Bit		
0	×	0	0	Unchanged
1	×	0	1	Unchanged
×	0	1	0	Cleared by Host
×	1	1	1	Set by Host

4.5 Socket and Copy Register (Address 206h in attribute memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive#	0	0	0	0
Write	0	0	0	Drive#	$\times$	$\times$	$\times$	$\times$

Reserved   This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive #   This bit indicates the drive number of the card for twin card configuration. X The socket number is ignored by the PC Card.

4.6 I/O Transfer Function

4.6.1 I/O Function

The I/O transfer to or from the PC Card can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal -IOIS16 is asserted by the PC Card. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the PC Card, the system must generate a pair of 8-bit references to access the word's even byte and odd byte. The PC Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the PC Card responds. The PC Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 4-6 I/O Function

Function Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	×	H	H	×	×	×	High Z	High Z
Byte Input Access (8 bits)	L	H	L	L	L	H	High Z	Even Byte
	L	H	L	H	L	H	High Z	Odd Byte
Byte Output Access (8 bits)	L	H	L	L	H	L	Don't Care	Even Byte
	L	H	L	H	H	L	Don't Card	Odd Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd Byte	Even Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd Byte	Even Byte
I/O Read Inhibit	H	×	×	×	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	×	×	×	H	L	High Z	High Z
High Byte Inout Only (8 bits)	L	L	H	×	L	H	Odd Byte	High Z
High Byte Output Only (8 bits)	L	L	H	×	H	L	Odd Byte	Don't Care

4.7 Common Memory Transfer Function

4.7.1 Common Memory Function

The common memory transfer to or from the PC Card can be either 8 or 16 bits. The PC Card permits both 8 and 16 bit accesses to all of its common memory addresses.

The PC Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the –WAIT signal at the start of the cycle.

Table 4-7 Common Memory Function

Function Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	×	H	H	×	×	×	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even Byte Odd Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even Byte Odd Byte
Word Read Access (16 bits)	H	L	L	×	L	H	Odd Byte	Even Byte
Word Write Access (16 bits)	H	L	L	×	H	L	Odd Byte	Even Byte
Odd Byte Read Only (8 bits)	H	L	H	×	L	H	Odd Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	×	H	L	Odd Byte	Don't Care

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4.8 IDE Mode I/O Transfer Function

4.8.1 IDE I/O Function

The PC Card can be configured in a True IDE Mode of operation. The PC Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. In this True IDE Mode the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode no Memory or Attribute Registers are accessible to the host.

Note: Removing and reinserting the PC Card while the host computer's power is on will reconfigure the PC Card to PC Card ATA mode from the original True IDE Mode. To configure the PC Card in True IDE Mode, the 50-pin socket must be power cycled with the PC Card inserted and -OE (output enable) asserted. The following table defines the function of the operations for the True IDE Mode.

Table 4-8 IDE Mode I/O Function

Function Mode	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	×	×	×	High Z	High Z
Standby Mode	H	H	×	×	×	High Z	High Z
Task File Write	H	L	1-7h	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd Byte in	Even Byte in
Data Register Read	H	L	0	L	H	Odd Byte out	Even Byte out
Control Register Write	L	H	6h	H	L	Don't Care	Control In
All Status Read	L	H	6h	L	H	High Z	Status Out

4.9 ATA Drive Register Set Definition and Protocol

The PC Card can be configured as a high performance I/O device through:

a. Standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary); 170h-177h, 376h-377h(secondary) with IRQ 14 (or other available IRQ).

b. Any system decoded 16 byte I/O block using any available IRQ.

c. Memory space.

The communication to or from the PC Card is done using the Task File registers which provide all the necessary registers for control and status information. The PCMCIA interface connects peripherals to the host using four register mapping methods. The following is a detailed description of these methods:

Table 4-9 I/O Configurations

	Standard Configurations			
Config Index	I/O or Memory	Address	Drive #	Description
0 & 8	Memory	0-F, 400-7FF	0	Memory Mapped
1 & 9	I/O	××0-××F	0	I/O Mapped 16 Contiguous Registers
2 & Ah	I/O	1F0-1F7, 3F6-3F7	0	Primary I/O Mapped Drive 0
2 &Ah	I/O	1F0-1F7, 3F6-3F7	1	Primary I/O Mapped Drive 1
3 & Bh	I/O	170-177, 376-377	0	Secondary I/O Mapped Drive 0
3 & Bh	I/O	170-177, 376-377	1	Secondary I/O Mapped Drive 1

Note: *Refer to Section 4.5 for Twin Card implementation.*

4.9.1 I/O Primary and Secondary address configurations

Table 4-10 Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Notes
0	1F(17)	0	0	0	0	Even RD Data	Even WR Data	1,2
0	1F(17)	0	0	0	1	Error Register	Features	1
0	1F(17)	0	0	1	0	Sector Count	Sector Count	
0	1F(17)	0	0	1	1	Sector No.	Sector No.	
0	1F(17)	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)	0	1	1	1	Status	Command	
0	3F(37)	0	1	1	0	Alt Status	Drive Control	
0	3F(37)	0	1	1	1	Drive Address	Reserved	

Note: 1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers which lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

2. A byte accesses to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

3. Address lines which are not indicated are ignored by the PC Card for accessing all the registers in this table.

4.9.2 Configurations I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the PC Card, the registers are accessed in the block of I/O space decoded by the system as follows:

Table 4-11 Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Feature	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

Note:

1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even than odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Address lines which are not indicated are ignored by the PC Card for accessing all the registers in this table.

4.9.3 Memory Mapped Addressing

When the PC Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as follows:

Table 4-12 Memory Mapped Decoding

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
1	0	×	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	×	0	0	0	1	1	Error	Features	2
1	0	×	0	0	1	0	2	Sector Count	Sector Count	
1	0	×	0	0	1	1	3	Sector No.	Sector No.	
1	0	×	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	×	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	×	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	×	0	1	1	1	7	Status	Command	
1	0	×	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	×	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	×	1	1	0	1	D	Dup. Error	Dup. Feature	2
1	0	×	1	1	1	0	E	Alt Status	Device Ctl	
1	0	×	1	1	1	1	F	Drive Address	Reserved	
1	1	×	×	×	×	0	8	Even RD Data	Even WR Data	3
1	1	×	×	×	×	1	9	Odd RD Data	Odd WR Data	3

Notes:

1. Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to address 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1Kbyte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space. Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PCMCIA socket adapters also have auto incrementing address logic

embedded within them. This address window allows these hosts and adapters to function efficiently. Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the PC Card. A word access to address at offset 8 will provide even data on the low-order byte of the data bus, along with odd data at offset 9 on the high-order byte of the data bus.

4.9.4 True IDE Mode Addressing

When the PC Card is configured in the True IDE Mode, the I/O decoding is as follows:

Table 4-13 True IDE Mode I/O Decoding

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0	Notes
1	0	0	0	0	Even RD Data	Even WR Data	
1	0	0	0	1	Error	Features	
1	0	0	1	0	Sector Count	Sector Count	
1	0	0	1	1	Sector No.	Sector No.	
1	0	1	0	0	Cylinder Low	Cylinder Low	
1	0	1	0	1	Cylinder High	Cylinder High	
1	0	1	1	0	Select Card/Head	Select Card/Head	
1	0	1	1	1	Status	Command	
0	1	1	1	0	Alt Status	Device Control	
0	1	1	1	1	Drive Address	Reserved	

4.10 ATA Registers

The following section describes the hardware registers used by the host software to issue commands to the CompactFlash device. These registers are often collectively referred to as the "task file."

Note: *In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address –1) using data bus lines (D15-D8) when –CE1 is high and –CE2 is low unless –IOIS16is high (not asserted) and an I/O cycle is being performed.*

4.10.1 Data Register (Address -1F0[170]; Offset 0,8,9):

The Data Register is a 16bit register, and it used to transfer data blocks between the PC Card data buffer and the Host. This register overlaps the Error Register.

The table below describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt   to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 3.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

Note:

Because of the overlapped register, access to the 1f1h, 171h or offset 1 are not defined for word (-CE2 = 0 and – CE1 = 0) operations. These accesses are treated as accesses to the Word Data Register.

The duplicated registers at offsets 8,9 and Dh have no restrictions on the operations that can be performed by the socket.

Data Register	-CE2	-CE1	A0	Offset	Data Bus
Word Data Register	0	0	×	0,8,9	D15-D0
Even Data Register	1	0	0	0,8	D7-D0
Odd Data Register	1	0	1	9	D7-D0
Odd Data Register	0	1	×	8,9	D15-D8
Error / Feature Register	1	0	1	1,Dh	D7-D0
Error / Feature Register	0	1	×	1	D15-D8
Error / Feature Register	0	0	×	Dh	D15-D8

4.10.2 Error Register (Address -1F1[171]; Offset 1, Dh Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15 –D8 during a write operation to offset 0 with –CE2 low and –CE1 high.

Bit 7 (BBK)   This bit is set when a Bad Block is detected.This bit is set when Error on
                          drive 1 (True IDE).

Bit 6 (UNC)   This bit is set when an Uncorrectable Read Error is encountered.

Bit 5   This bit is 0.

Bit 4 (IDNF)   The requested sector ID is in error or cannot be found. This bit is 0

Bit 3   This bit is 0.

Bit 2 (Abort)   Abort=1 This bit is set if the command has been aborted because of a CompactFlash
                          Storage Card status condition (Write Fault, Invalid Parameter, etc) or when an invalid
                          command has been issued.

Bit 1   This bit is 0.

Bit 0 (AMNF)   This bit is set in case of a general error. (DMA transfer Error)

4.10.3 Feature Register (Address -1F1[171]; Offset 1, Dh Write Only):

This register provides information regarding features of the PC Card that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and –CE1 high.

4.10.4 Sector Count Register (Address -1F2[172]; Offset 2):

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the PC Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request

4.10.5 Sector Number (LBA 7-0) Register (Address -1F3[173]; Offset 3):

This register contains starting sector number or bits 7-0 of the Logical Block Address (LBA) for any PC Card data access for the subsequent command.

4.10.6 Cylinder Low (LBA 15-8) Register (Address -1F4[174]; Offset 4):

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

4.10.7 Cylinder High (LBA 23-16) Register (Address -1F5[175]; Offset 5):

This register contains the high order 8 bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

4.10.8 Drive/Head (LBA 27-24) Register (Address -1F6[176]; Offset 6):

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defines as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7   This bit is set to 1.

Bit 6 (LBA)   LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA = 1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:

         LBA7-LBA0:   **Sector Number Register D7-D0.**
         LBA15-LBA8:   **Cylinder Low Register D7-D0.**
         LBA23-LBA16:   **Cylinder High Register D7-D0.**
         LBA27-LBA24:   **Drive/Head Register HS3-HS0.**

Bit 5   1 This bit is set to 1.

Bit 4 (DRV)   DRV is the drive number. When DRV 0, drive (card) 0 is selected. When DRV = 1,drive (card) 1 is selected. The PC Card is set to be Card 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register.

Bit 3 (HS3)   When operating in the Cylinder, Head, Sector mode, this is bit3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2)   When operating in the Cylinder, Head, Sector mode, this is bit2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1)   When operating in the Cylinder, Head, Sector mode, this is bit1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0)   When operating in the Cylinder, Head, Sector mode, this is bit0 of the head number. It is Bit 24 in the Logical Block Address mode

4.10.9 Status & Alternate Status Register (Address -1F7[177]&3F6[376]; Offset 7, Eh):

These registers return the PC Card status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits is described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY)   The busy bit is set when the PC Card has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY)   RDY indicates whether the device is capable of performing PC Card operations. This bit is cleared at power up and remains cleared until the PC Card is ready to accept a command.

Bit 5 (DWF)   This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC)   This bit is set when the PC Card is ready. This bit is cleared at power up.

Bit 3 (DRQ)   The Data Request is set when the PC Card required and that information be transferred either to or from the host through the Data register.

Bit 2 (CORR)   This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.
Bit 1   This bit is always set to 0.

Bit 0 (ERR)   This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

4.10.10 Device Control Register (Address –3F6[376]; Offset Eh):

This register is used to control the PC Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
×	×	×	×	1	SW Rst	-IEn	0

Bit 7   This bit is an X (don't care).

Bit 6   This bit is an X (don't care).

Bit 5   This bit is an X (don't care).

Bit 4   This bit is an X (don't care).

Bit 3   This bit is ignored by the PC Card.

Bit 2(SW Rst)   This bit set to 1 in order to force the PC Card to perform an AT Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration Registers (4.3.2-to 4.3.5) as hardware Reset does. The Card remains in Reset until this bit is reset to "0".

Bit 1   The Interrupt Enable bit enables interrupts when the bit is 0 (-IEn=0), interrupts from the PC Card are disable. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 1 at power on and Reset.

Bit 0   This bit ignored by the PC Card.

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4.10.11 Card (Drive) Address Register (Address -3F7[377]; Offset Fh):

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register nit be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follow:

D7	D6	D5	D4	D3	D2	D1	D0
$\times$	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7   This bit is unknown.

Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the PC Card. Following are some possible solutions to this problem for the PCMCIA implementation:

1.Locate the PC Card at a non –conflicting address, i.e. Secondary address (377h) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses.

2.Do not install a Floppy and a PC Card in the system at the same time.

3.Implement a socket adapter which can be programmed to (conditionally) tri-state D7 of I/O address 3F7h/377h when a PC Card is installed and conversely to tri-state D6-D0 of I/O address 3F7h/377h when a floppy controller is installed.

4.Do not use the PC Card's Drive Address register. This may be accomplished by either If possible, program the host adapter to enable only I/O address 1F0h-1F7h, 3F6h (or 170-177h, 176h) to the PC Card or If provided use an additional Primary/Secondary configuration in the PC Card which does not respond to accesses to I/O location 3F7h and 377h with either of these implementation, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG)   This bit is 0 when a write operation is in progress, otherwise, it is 1.

Bit 5 (-HS3)   This bit is the negation of bit 3 in the Drive/Head register.

Bit 4 (-HS2)   This bit is the negation of bit 2 in the Drive/Head register.

Bit 3 (-HS1)   This bit is the negation of bit 1 in the Drive/Head register.

Bit 2 (-HS0)   This bit is the negation of bit 0 in the Drive/Head register.

Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected

Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

4.11 ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the PC Cards. Command are issued to the PC Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 6-1) of command acceptance, all dependent on the host not issuing commands unless the PC Card is not busy (BSY = 0).

4.11.1 Vendor Unique Command

Bit->	7	6	5	4	3	2	1	0
Command (7)				EFH				
C/D/H (6)		×		Drive		×		
Cylinder High (5)				×				
Cylinder Low (4)				×				
Sec Number (3)				×				
Sec Count(2)				Config				
Feature (1)				Feature				

A Vendor unique command is setting F0h as Feature REGISTER of a SET FEATURE COMMAND, and is executed. Moreover, each Vendor unique command is processed with the setting value of Config.

Set Features Command(EF h) ConfigFeature Value = F0h

Config Value	Command Name	Description
C0	Physical Read	Read from physical page on flash memory.
C1	Physical Write	Write data to physical page on flash memory.
C2	Physical Block Erase	Erase physical block on flash memory.
C3	Set SG Control Table	Set SG Control Table for initializing Flash Memory
C4	Flash initialize	Executing Flash Memory initializing.
C5	Change Information CIS/DID	Changing Data of CIS/DID.
C6	Get Flash Information	Getting flash Memory information. (Structure of Block number and Page number.)
C7	Get Firmware Revision	Getting Firmware Revision.
C8	Get Flash ID Information	Getting flash information of Maker ID and Device ID.

Note1

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4.11.2 Physical Read Sector

Bit->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	×			Drive	×			
Cylinder High (5)	Page No High							
Cylinder Low (4)	Page No Low							
Sec Number (3)	Chip No (0-31)							
Sec Count(2)	C0h							
Feature (1)	F0h							

Features code F0h enables the host to configure the card to test card function. The host sets a value C0h in the Sector Count register that is permission physical sector access.

The Physical Read Sector command performs similarly to the Read Sector(s) command except that it returns 528 bytes from physical sector (flash page). During a Physical Read Sector command, the PC Card does not check the ECC bytes to determine if there has been a data error. Only single sector Read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 16 bytes of spare data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is Developer's test.

●   Input parameter

Cylinder High Low = The page address within a memory chip. (0-　)

Sector Number = Memory chip number. (0-31)

●   The output parameter at the time of a normal end

Status Register = 50h

●   The output parameter at the time of an unusual end.

An address is too large.

Status Register = 51h

Error Register = 10h(ID Not Found)

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4.11.3 Physical Write Sector

Bit->	7	6	5	4	3	2	1	0
Command (7)				EFH				
C/D/H (6)	×			Drive		×		
Cylinder High (5)				Page No High				
Cylinder Low (4)				Page No Low				
Sec Number (3)				Chip No (0-31)				
Sec Count(2)				Ch				
Feature (1)				F0h				

The Physical Write Sector command performs similarly to the Write Sector(s) command except that it writes 528 bytes of data instead of 512 bytes. During a Physical Write Sector command, the PC Card does not check the ECC bytes to determine if there has been a data error. Only single page Write operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 16 bytes of spare data transferred in byte mode. This command has the same protocol as the write Sector(s) command. Use of this command is Developer's test.

●   Input parameter

Cylinder High Low = The page address within a memory chip. (0-)

Sector Number = Memory chip number. (0-31)

●   The output parameter at the time of a normal end

Status Register = 50h

●   The output parameter at the time of an unusual end.

An address is too large.

Status Register = 51h

Error Register = 10h(ID Not Found)

●   Write fault.

Status Register = 71h(Write fault)

Error Register = 80h(Bad Block Detected)

4.11.4 Physical Erase Block

Bit->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)		×		Drive		×		
Cylinder High (5)	Block No High							
Cylinder Low (4)	Block No Low							
Sec Number (3)	Chip No (0-31,FFh)							
Sec Count(2)	Ch							
Feature (1)	F0h							

CF which a command was taken in does elimination toward physical Block of the specified chip Number.
It is the erase of only one block. A Sec Number of FFh requests all block Erase.
Block No is Block Address in a tip simple substance.

4.11.5 Set SG(Sector Group)Control Table

Bit->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)		×		Drive		×		
Cylinder High (5)	The number of link blocks							
Cylinder Low (4)	The number of spared part blocks							
Sec Number (3)	The number of updated part blocks							
Sec Count(2)	C3h							
Feature (1)	F0h							

A garbage collection is performed. This Command must be executed before Initialize Flash Memory Command.

4.11.6 Initialize Flash Memory

Bit->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	×			Drive	×			
Cylinder High (5)	×							
Cylinder Low (4)	Number of mounted Flash Memory							
Sec Number (3)	Erase Flash Switch							
Sec Count(2)	C4h							
Feature (1)	F0h							

This command checks all flash memory, and after then, write information of control. The blank check of all the mounting flash memories is done, and Write/Read/Compare/Erase is done, and writing a control table are made (initialization to do after mounting).
Sec Number :When This Value is FFh, Erase block of all the mounting flash memories.

Note. Before this Command execution, all blocks must be erased. After this Command execution, it must execute the Write CIS/DID Command (Change Card Information).

Error return value (Sec Number)

Error Value	Description
00h	Normalcy End: it is Sec Number =00h.
01h	All flash chip is not recognized by ID read command.
02h	Block 0 or Block 1 erase check error.
03h	Block 0 or Block 1 write/read check error.
04h	CIS/DID Write page error
05h	Link info writes error or **SG ctbl** (The table of control information) build up error.

4.11.7 Change Card Information

Bit->	7	6	5	4	3	2	1	0
Command (7)				EFH				
C/D/H (6)		×		Drive		×		
Cylinder High (5)				Interleave Mode				
Cylinder Low (4)				FAT Analysis Mode				
Sec Number (3)				×				
Sec Count(2)				C5h				
Feature (1)				F0h				

This command change card information. As for doing action, writing of CIS/DID and Flash Information to page of the fixation, others is the same protocol as Write Sector Command the elimination of the fixed block. But Flash information currently written in is inherited, without updating.

Format of writes data (format)

Byte	Description
0-255	CIS(Vendor Unique)
256-511	Drive Identify Information(Vendor Unique)

Special specification(Note)

Specification	Set Register	Function
Interleave	Cylinder High	2F:Enable, 1Fh:Disable
FAT Analysis	Cylinder Low	FA:Enable, F0h:Disable

Data of Special specification are written on Flash memory (1Byte). That location is Page No.1 of Block No.0. Data after 2 byte is invalid.

Default is Disable (FFh).

Note: This specification is not supported now.

4.11.8 Get Flash chip Information

Bit->	7	6	5	4	3	2	1	0
Command (7)				EFH				
C/D/H (6)		×		Drive		×		
Cylinder High (5)				×				
Cylinder Low (4)				×				
Sec Number (3)				×				
Sec Count(2)				C6h				
Feature (1)				F0h				

This command checks connecting flash chip information. The PC Card sets Sector Number Register to Page number per block, Cylinder Low Register to Block number LSB, Cylinder High Register to Block number MSB.

4.11.9 Get Firmware Information

Bit->	7	6	5	4	3	2	1	0
Command (7)				EFH				
C/D/H (6)		×		Drive		×		
Cylinder High (5)				×				
Cylinder Low (4)				×				
Sec Number (3)				×				
Sec Count(2)				C7h				
Feature (1)				F0h				

This command checks the Firmware Revision. The PC Card sets Sector Number Register to firmware version. Firmware Revision A.B

Return parameter: Sector Number = Firmware Revision Byte (A).

Cylinder Low = Firmware Revision Byte (B).

4.11.10 Get Flash ID Information

Bit->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	×			Drive	×			
Cylinder High (5)	×							
Cylinder Low (4)	×							
Sec Number (3)	×							
Sec Count(2)	C8h							
Feature (1)	F0h							

This command checks connecting flash chip information. The PC Card sets Sector Number Register to mounting chip number, Cylinder Low Register to maker ID, Cylinder High Register to device ID.

4.12 Card Information Structure(Default)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
000h	01	CISTPL_DEVICE								Device Info Tuple	Tuple Code
002h	04									Link is 4bytes	Link to next tuple
004h	DF	Device Type Code Dh=I/O			W 1		Speed 7h				I/O device, No Write Protects,	Device ID WPS, Speed
006h	4A	X		9h				2h		Device Speed = 400ns	
008h	01	Device Size								2Kbyte of address Space	Device Size
00Ah	FF	List End Marker								End of Devices	End Marker
00Ch	1C	CISTPL_DEVICE_OC								Other Condition Device Info Tuple	Tuple Code
00Eh	04									Link is 4bytes	Link to next tuple
010h	02	0	Reserved, 0				VccU		M	3.3V Vcc Operation	OC Info
012h	D9	Device Type Code Dh=I/O			W 1		Speed 1h			I/O device, No Write Protects, Device Speed=250ns	Device ID WPS, Speed
014h	01	Device Size								2Kbyte of address Space	Device Size
016h	FF	List End Marker								End of Devices	End Marker
018h	18	CISTPL_JEDEC_C								JEDEC ID Common Mem	Tuple Code
01Ah	02									Link is 2bytes	Link to next tuple
01Ch	DF	PCMCIA Manufacture's ID								First Byte of JEDEC ID	JEDEC ID of Device 1
01Eh	01	PCMCIA Code for PC Card-ATA No Vpp Required								Second Byte of JEDEC ID	JEDEC ID
020h	20	CISTPL_MANFID								Manufacture ID String	Tuple Code
022h	04									Link is 4bytes	Link to next tuple
024h	CE	PC Card Manufacture's ID Code									TPLMID_MANF
026h	00										TPLMID_MANF
028h	00	Manufacture Information									TPLMID_CARD
02Ah	00										TPLMID_CARD
02Ch	15	CISTPL_VERS_1								Level 1 Version/Product Information	Tuple Code
02Eh	20									Link is 20bytes	Link to next tuple

030h	04	Major Version Number	PCMCIA 2.1	TPLLV1_MAJOR
032h	01	Minor Version Number	JEIDA 4.2	TPLLV1_MINOR
034h	53	Manufacture Information	Name of Manufacture	String 1
036h	41			
038h	4D			
03Ah	53			
03Ch	55			
03Eh	4E			
040h	47		"SAMSUNG"	
042h	20			
044h	20			
046h	20			
048h	20			
04Ah	20			
04Ch	20			
04Eh	00	End of Manufacture Information	Null Terminator	End String 1
050h	53	Product Information	Name of Product	String 2
052h	43			
054h	46			
056h	44			
058h	2D			
05Ah	56			
05Ch	45		"SCFD-VER1.0"	
05Eh	52			
060h	31			
062h	2E			
064h	30			
066h	20			
068h	20			
06Ah	00	End of Product Information	Null Terminator	End String 2
06Ch	00	End of CIS Revision Number	Null Terminator	
06Eh	FF	List End Marker		End Marker
070h	21	CISTPL_FUNCID	Function ID Tuple	Tuple Code
072h	02		Link is 2bytes	Link to next tuple

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074h	04	IC Card Function Code								Fixed Disk Function	TPLFID_FUNCTION
076h	01	RFU, 0						R	P	System Initialization Bit Mask, Power-On-Self Test	TPLFID_SYSINIT
078h	22	CISTPL_FUNCE								Function Extention Tuple	Tuple Code
07Ah	02									Link is 2bytes	Link to next tuple
07Ch	01	Disk Function Extension Tuple Type								Disk Device Interface	TPLFE_TYPE
07Eh	01	Interface Type Code								PC Card-ATA Interface	TPLFE_DATA
080h	22	CISTPL_FUNCE								Function Extention Tuple	Tuple Code
082h	03									Link is 3bytes	Link to next tuple
084h	02	Disk Function Extension Tuple Type								Disk Device Interface	TPLFE_TYPE
086h	0C	RFU			U	S	V			Silicon/Rotating, ID/SN is unique,	TPLFE_DATA
088h	0F	R	I	E	N	P3	P2	P1	P0	Auto, Idle, Standby, Sleep Mode supported	TPLFE_DATA
08Ah	1A	CISTPL_CONFIG								Configuration Tuple	Tuple Code
08Ch	05									Link is 5bytes	Link to next tuple
08Eh	01	RFSZ		RMSZ			RASZ			Size of Fields Byte	TPCC_SZ
090h	03	TPCC_LAST								Entry Index 03h	Last entry of Configuration table
092h	00	TPCC_RADR								Configuration Registers are located at 200h	Location of Config Registers
094h	02	TPCC_RADR									
096h	0F	RFU			S	P	C	I		4 Configuration Registers are present	TPCC_RMSK
098h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
09Ah	08									Link is 8bytes	Link to next tuple
09Ch	C0	I	D	Configuration Entry Number						Memory Mapped I/O, D: Default Configuration, I: Interface Byte Follows	TPCE_INDX

09Eh	C0	MW	R	WP	BV	Interface Type			Memory Only Interface, Bvd & WP not used, RDY/BSY & Wait used for Memory Cycle	TPCE_IF
0A0h	A1	M	MS		IRQ	IO	T	Power	Vcc power-description structure only, MS: Single 2-byte length specified M: Misc field structure is present	TPCE_FS
0A2h	01	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating Supply Voltage, No Extension	Power Parameters for Vcc
0A4h	55	X		Ah			5h			Vcc Noninal is 5V	Vcc Nominal Value
0A6h	08	Length in 256 bytes pages(LSB)								Length of Mem Space is 2KB	TPCE_MS Length LSB
0A8h	00	Length in 256 bytes pages(MSB)								Start at 0 on Card	TPCE_MS Length MSB
0AAh	20	X	R	P	R	A	Twin			Power Down	TPCE_MI
0ACh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
0AEh	06									Link is 6bytes	Link to next tuple
0B0h	00	I	D	Configuration Entry Number							TPCE_INDX
0B2h	01	M	MS		IRQ	IO	T	Power		Vcc power-description structure only	TPCE_FS
0B4h	21	R	DI	PI	AI	SI	HV	LV	NV	Maximum Current required averaged over 10ms, Nominal Operating Supply Voltage, With Extension	TPCE_PD
0B6h	B5	X		6h			5h			1V x 3	Vcc Nominal Value
0B8h	1E	X		1Eh(30d)						Vcc Nominal is 3.3V	
0BAh	4D	X		9h			5h			Peak I is 45mA	Peak I Value

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0BCh	1B	CISTPL_CFTABLE_ENTRY							Configuration Entry Tuple	Tuple Code
0BEh	0A								Link is 10bytes	Link to next tuple
0C0h	C1	I	D	Configuration Entry Number					I/O Mapped Contiguous 16 Registers Configuration, D: Default Configuration, I: Interface Byte Follows	TPCE_INDX
0C2h	41	W	R	P	B	Interface Type			I/O Interface, Bvd & WP not used, RDY/BSY active, Wait not used for memory access	TPCE_IF
0C4h	99	M	MS		IRQ	IO	T	Power	Misc & IRQ field are present, Vcc power-description structure only	TPCE_FS
0C6h	01	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating supply Voltage	TPCE_PD
0C8h	55	X	Ah			5h			Vcc Nominal is 5V	Vcc Nominal Value
0CAh	64	R	Bus 16/8	I/O AddrLines					Support 16/8 bit I/O access, I/O Address Lines are 16	TPCE_IO
0CCh	F0	S	P	L	M	V	B	I	N	IRQ Sharing S: Share Logic active, P: Pulse IRQ supported, L: Level IRQ supported, M: Bit Mask of IRQ	TPCE_IR
0CEh	FF								IRQ Levels to be routed 0-7 recommended	TPCE_IR Mask Extension
0D0h	FF								IRQ Levels to be routed 8-15 recommended	TPCE_IR Mask Extension
0D2h	20	X	R	P	RO	A	T		Power Down supported	TPCE_MI

Address	Value	Bit Fields	Description	Field
0D4h	1B	CISTPL_CFTABLE_ENTRY	Configuration Entry Tuple	Tuple Code
0D6h	06		Link is 6bytes	Link to next tuple
0D8h	01	I D Configuration Entry Number		TPCE_INDX
0DAh	01	M MS IRQ IO T Power	Vcc power-description structure only	TPCE_FS
0DCh	21	R DI PI AI SI HV LV NV	Nominal Operating supply Voltage, Maximum Current required averaged over 10ms	TPCE_PD
0DEh	B5	X 6h 5h	1V x 3	Vcc Nominal Value
0E0h	1E	X 1Eh(30d)	Vcc Nominal is 3.3V	
0E2h	4D	X 9h 5h	Peak I is 45mA	Peak I Value
0E4h	1B	CISTPL_CFTABLE_ENTRY	Configuration Entry Tuple	Tuple Code
0E6h	0F		Link is 15bytes	Link to next tuple
0E8h	C2	I D Configuration Entry Number		TPCE_INDX
0EAh	41	W R P B Interface Type	I/O Interface, Bvd & WP not used, RDY/BSY active, Wait not used for memory access	TPCE_IF
0ECh	99	M MS IRQ IO T Power	Misc & IRQ field are present, Vcc power-description structure only	TPCE_FS
0EEh	01	R DI PI AI SI HV LV NV	Nominal Operating supply Voltage	TPCE_PD
0F0h	55	X Ah 5h	Vcc Nominal is 5V	Vcc Nominal Value

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0F2h	EA	R	Bus 16/8		I/O AddrLines				I/O range description, Support 16/8 bit I/O access, A 1 Kbyte I/O address space	TPCE_IO
0F4h	61	Size of length	Size of address	Number of I/O Address Ranges					Length is 1 byte long, Address is 2 byte long, 1 I/O Address Range Description field	I/O Range Description Byte
0F6h	F0	Start of I/O Address Block First(LSB)								
0F8h	01	Start of I/O Address Block First(MSB)								
0FAh	07	First I/O Range Length								
0FCh	F6	Start of I/O Address Block Second(LSB)								
0FEh	03	Start of I/O Address Block Second(MSB)								
100h	01	Second I/O Range Length								
102h	EE	S	P	L	M	V	B	I	N	IRQ Sharing S: Share Logic active, P: Pulse IRQ supported, L: Level IRQ supported, V: Vendor-Specific supported, B: Bus-Error supported, I: I/O-check supported	TPCE_IR
104h	20	X	R	P	RO	A	T			Power Down supported	TPCE_MI
106h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
108h	06									Link is 6bytes	Link to next tuple
10Ah	02	I	D	Configuration Entry Number							TPCE_INDX
10Ch	01	M	MS		IRQ	IO	T	Power		Vcc power-description structure only	TPCE_FS
10Eh	21	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating supply Voltage,	TPCE_PD

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									Maximum Current required averaged over 10ms	
110h	B5	X	6h			5h			1V x 3	Vcc Nominal Value
112h	1E	X	1Eh(30d)						Vcc Nominal is 3.3V	
114h	4D	X	9h			5h			Peak I is 45mA	Peak I Value
116h	1B	CISTPL_CFTABLE_ENTRY							Configuration Entry Tuple	Tuple Code
118h	0F								Link is 15bytes	Link to next tuple
11Ah	C3	I	D	Configuration Entry Number						TPCE_INDX
11Ch	41	W	R	P	B	Interface Type			I/O Interface, Bvd & WP not used, RDY/BSY active, Wait not used for memory access	TPCE_IF
11Eh	99	M	MS		IRQ	IO	T	Power	Misc & IRQ field are present, Vcc power-description structure only	TPCE_FS
120h	01	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating supply Voltage	TPCE_PD
122h	55	X	Ah			5h			Vcc Nominal is 5V	Vcc Nominal Value
124h	EA	R	Bus 16/8		I/O AddrLines				I/O range description, Support 16/8 bit I/O access, A 1 Kbyte I/O address space	TPCE_IO
126h	61	Size of length	Size of address	Number of I/O Address Ranges					Length is 1 byte long, Address is 2 byte long, 1 I/O Address Range Description field	I/O Range Description Byte
128h	70	Start of I/O Address Block First(LSB)								
12Ah	01	Start of I/O Address Block First(MSB)								
12Ch	07	First I/O Range Length								

Addr	Data									Description	Field
12Eh	76	Start of I/O Address Block Second(LSB)									
130h	03	Start of I/O Address Block Second(MSB)									
132h	01	Second I/O Range Length									
134h	EE	S	P	L	M	V	B	I	N	IRQ Sharing S: Share Logic active, P: Pulse IRQ supported, L: Level IRQ supported, V: Vendor-Specific supported, B: Bus-Error supported, I: I/O-check supported	TPCE_IR
136h	20	X	R	P	RO	A		T		Power Down supported	TPCE_MI
138h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
13Ah	06									Link is 6bytes	Link to next tuple
13Ch	03	I	D	Configuration Entry Number							TPCE_INDX
13Eh	01	M	MS	IRQ	IO	T	Power			Vcc power-description structure only	TPCE_FS
140h	21	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating supply Voltage, Maximum Current required averaged over 10ms	TPCE_PD
142h	B5	X	6h				5h			1V x 3	Vcc Nominal Value
144h	1E	X	1Eh(30d)							Vcc Nominal is 3.3V	
146h	4D	X	9h				5h			Peak I is 45mA	Peak I Value
148h	14	CISTPL_NO_LINK								No Link to Common Memory	Tuple Code
14Ah	00	No Bytes Following								Link Length is 0 byte	Link to next tuple
14Ch	FF	End of CIS Tuple Chain								End of CIS	Tuple Code

4.13 Example test of production

(1) Modules check.
(2) Set feature Command code C4

    Check Flash Memory.   (Initialize Flash Memory)
    Initialization Table.   (Initialize Flash Memory)
    Managed table creation.   (Initialize Flash Memory)

(3) Set feature Command code C5

    Write CIS/DIDFLASH.   (Change Information)

(4) Card check. (function)

Physical Disk Format	*ATAINIT*DOS	Set Parameter
Logical Disk Format	FORMATDOS	FAT16,FAT32,NTFS etc.
Read/Write check	SCANDISKDOS	

Note :   *ATAINIT is a Card Wizard utility that create a DOS partition on the FlashDisk card.*
        ATAINIT program(the System Soft Corp FDISK utility).

4.14 Load of CIS Card Information Structure DID Drive Identify Data

- The foundations of CIS are defined as the firmware of ARM7TDMI. (Definition of only 5V power supply.)
- When effective data as CIS does not have data in head block of a flash or flash is not mounted, data
  defined as the firmware is loaded as CIS.
- When there is CIS developed to the flash (After CIS and DID are written), its data become effective,
  CIS is read from a flash.
- DID is not defined in first stage.
- The write of CIS/DID and the code of rewriting are put on the first page of first block of a flash, and
  access to other blocks is not performed (management TBL etc. is not changed).
- CIS/DID needs to be rewritten with the specification of a card.
- Concept figure (CIS/DID Load action).

4.15 Power On Error

Specification when an internal initialization error happens is explained at the time of power-supply starting.
When failing in initialization, the following bit is set as ERROR Register and status is set to RDY.

ERROR Register bit	Description
Bit1	flash ROM read ID error or reset error
Bit3	CIS read error (error occurred even when CIS in ROM is used)
Bit5	link block read error

5 ELECTRICAL DATA

OVERVIEW

In this section, S3C49F9X electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings

— Recommended operating conditions

— Thermal characteristics

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply voltage	-0.3 to $+7.0$	V
V_{IN}	Input voltage	-0.3 to $V_{DD} + 0.3$	V
I_{IN}	DC input current	-10	mA
T_{STG}	Storage temperature	-40 to $+125$	°C

Table 5-2. Recommended Operating Conditions

Symbol	Parameter		Ratings	Unit
V_{DD}	DC supply voltage	5 V	4.75 to $+5.25$	V
		3.3 V	3.0 to 3.6	V
Ta	Storage temperature		-40 to $+85$	°C

Table 5-3. Thermal Characteristics

Symbol	Parameter	Value	Unit
θja	Thermal impedance - junction to ambient plastic 144-pin LQFP	57	°C /W

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Table 5-4. D.C. Electrical Characteristics

(T_A = 0 to 70 $°$C, V_{DD} = 3.3 V $\pm$ 0.3 V)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	High level input voltage	CMOS		2.0			V
V_{IL}	Low level input voltage	CMOS				1.0	V
V_T	Switching threshold	CMOS			1.4		V
V_{T+}	Switching trigger, positive-going threshold	CMOS				2.0	V
V_{T-}	Switching trigger, negative-going threshold	CMOS		1.0			V
I_{IH}	High level input current	Input buffer	$V_{IN} = V_{DD}$	−10		10	uA
		Input buffer with pull-up		10	30	60	
I_{IL}	Low level input current	Input buffer	$V_{IN} = V_{SS}$	−10		10	uA
		Input buffer with pull-up		−160	−30	−10	
V_{OH}	High level output voltage	Type 4 [1]	$I_{OH} = -4$ mA	2.4			V
		Type 4 [2]	$I_{OH} = -8$ mA				
		Type 4 [3]	$I_{OH} = -16$ mA				
V_{OL}	Low level output voltage	Type 4 [1]	$I_{OH} = 4$ mA			0.4	V
		Type 4 [2]	$I_{OH} = 8$ mA				
		Type 4 [3]	$I_{OH} = 16$ mA				
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}		−10		10	uA
I_{DD}	Maximum operating current	$V_{DD} = 5.0$ V, $f_{MCLK} = 20$ MHz			30	40	mA
Iidle	Idle current					20	mA
Ids	Stop current					30	uA

NOTES:
1.   4 mA drive output PAD.
2.   8 mA drive output PAD.
3.   16 mA drive output PAD.

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Table 5-4. D.C. Electrical Characteristics

$(T_A = 0$ to $70\,°C, V_{DD} = 5\,V \pm 5\,\%)$

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	CMOS		3.5			V
		TTL		2.0			
V_{IL}	Low level input voltage	CMOS				1.5	V
		TTL				0.8	
V_T	Switching threshold	CMOS			2.5		V
		TTL			1.4		
V_{T+}	Switching trigger, positive-going threshold	CMOS				4.0	V
		TTL				2.0	
V_{T-}	Switching trigger, negative-going threshold	CMOS			1.0		V
		TTL			0.8		
I_{IH}	High level input current	Input buffer	$V_{IN} = V_{DD}$	−10		10	uA
		Input buffer with pull-up		10	50	100	
I_{IL}	Low level input current	Input buffer	$V_{IN} = V_{SS}$	−10		10	uA
		Input buffer with pull-up		−100	−50	−10	
V_{OH}	High level output voltage	Type 4 [1]	$I_{OH} = −4$ mA	2.4			V
		Type 4 [2]	$I_{OH} = −8$ mA				
		Type 4 [3]	$I_{OH} = −16$ mA				
V_{OL}	Low level output voltage	Type 4 [1]	$I_{OH} = 4$ mA			0.4	V
		Type 4 [2]	$I_{OH} = 8$ mA				
		Type 4 [3]	$I_{OH} = 16$ mA				
I_{OZ}	Tri-state output leakage current		$V_{OUT} = V_{SS}$ or V_{DD}	−10		10	uA
I_{DD}	Maximum operating current		$V_{DD} = 5.0$ V, $f_{MCLK} = 20$ MHz		60	70	mA
Iidle	Idle current					35	mA
Ids	Stop current					60	uA

NOTES:
1.   4 mA drive output PAD.
2.   8 mA drive output PAD.
3.   16 mA drive output PAD.

6 MECHANICAL DATA

OVERVIEW

The S3C49F9X disk controller is available in a 100-pin TQFP package (Samsung part number 100-TQFP-1414)/
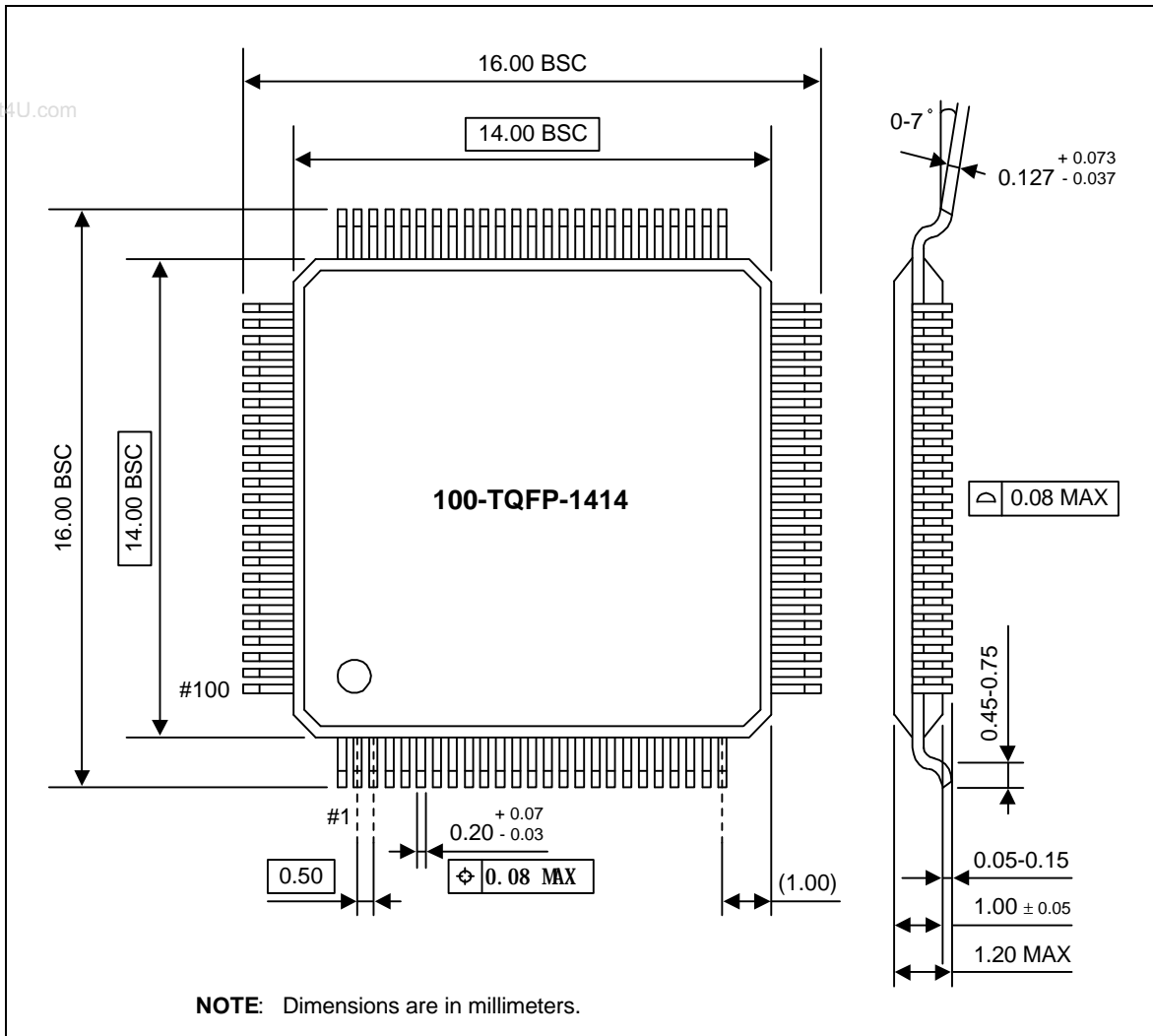
Figure 6-1. 100-TQFP-1414 Package Dimension
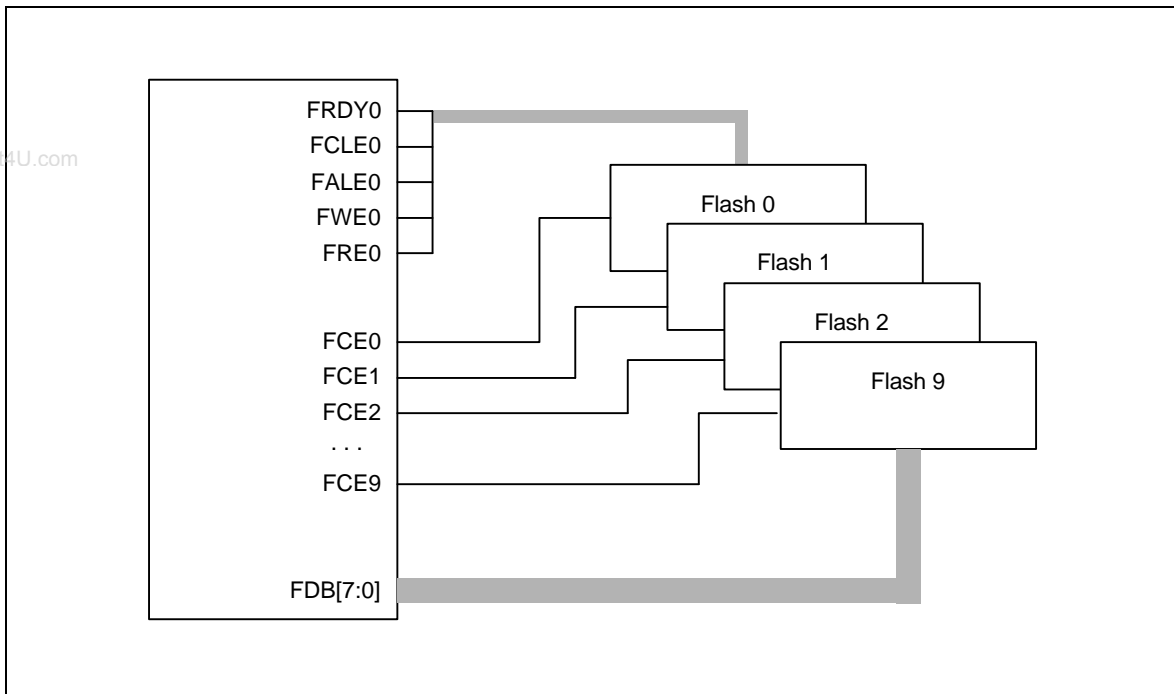
7 APPLICATION NOTE

FLASH MEMORY CONNECTION

Figure 7-1. Case of Using the S3C49F9X